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PERFORMANCE SPECIFICATION

CAPACITORS, FIXED, CERAMIC DIELECTRIC, HIGH RELIABILITY, DISCOIDAL, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the requirements for high reliability, discoidal, ceramic dielectric, fixed capacitors. This specification provides for two levels of product requirements: Class B and class S. Capacitors furnished to the requirements of this specification are intended for use in Radio Frequency/Electromagnetic Interference (RFI/EMI) suppression filters covered by MIL-PRF-28861.

1.2 Classification. Discoidal capacitors are classified into one of the following reliability levels as specified.

1.2.1 Product level. Two product levels of discoidal capacitors are provided for in this specification. The product level is identified by a single letter in accordance with table I:

TABLE I. Product level.

Symbol	Level
B	Class B
S	Class S

a. Class B - Class B is the base product level of this specification and is intended for all applications except for space applications. Class B discoidal capacitors are those which have been subjected to and passed all applicable requirements, tests, and inspections detailed herein, including in-process inspection and conformance inspection requirements for Class B.

b. Class S - Class S is the highest product level of this specification and is intended for space applications. Class S discoidal capacitors are those which have been subjected to and passed all applicable requirements, tests, and inspections detailed herein, including in-process inspection and conformance inspection requirements for Class S.

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime ATTN: VAT, Post Office Box 3990, Columbus, OH 43218-3990 or e-mailed to capacitorfilter@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.daps.dla.mil.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of the documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications. standards. and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-28861 - Filters and Capacitors, Radio Frequency/Electromagnetic Interference Suppression, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Test Method Standard Electronic and Electrical Component Parts.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

ELECTRONIC COMPONENTS ASSOCIATION (ECA)

EIA/ECA-469 - Standard Test Method for Destructive Physical Analysis (DPA) of High Reliability Ceramic Monolithic Capacitors.

(Copies of these documents are available from http://www.global.ihs.com or Global Engineering Documents, Attn: Customer Service Department, 15 Inverness Way East, Englewood CO 80112-5776.)

THE INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS INC. (IPC)

J-STD-006 - Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications.

(Copies of these documents can be ordered online at www.ipc.org or from the Institute for Interconnecting and Packaging Electronic Circuits (IPC, INC.), 2215 Sanders Road, Suite 200 South, Northbrook, IL 60062.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Product levels. Two product levels of capacitors are provided for in this specification, class S and class B. Class S is the highest product level of this specification and is intended for space applications.

3.2 Materials. The materials shall be as specified herein. However, when a definite material is not specified, a material shall be used which will enable the discoidal capacitors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be classified as a guaranty of the acceptance of the finished product.

3.3 Documentation of individual discoidal capacitors. Manufacturers of filters built in accordance with MIL-PRF-28861 shall specify the requirements of individual discoidal capacitors that shall include, but is not limited to, the following types of performance requirements:

a. Physical dimensions and terminations (see 3.6).

b. Dielectric constant (see 3.4).

c. Minimum dielectric thickness (see 3.4.1).

d. Electrical characteristics:

(1) Voltage rating (see 3.4.1).

(2) Capacitance and tolerance (see 3.8).

(3) Dissipation factor (see 3.9).

(4) Insulation resistance (see 3.11).

(5) Voltage-temperature limits (see 3.18).

3.4 Dielectric parameters. Capacitors supplied to this specification shall meet voltage temperature requirements of 3.18.

3.4.1 Dielectric thickness. Capacitors supplied to this specification shall have a minimum dielectric thickness of 8 mil (0.020 mm) for capacitors with ratings of 50 volts and below or 1.0 mil (0.025 mm) for capacitors with ratings above 50 volts. Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness by more than 50 percent.

3.5 Electrode parameters. Nickel or copper electrodes shall not be used in capacitors supplied to this specification.

3.6 Physical dimensions and terminations. The discoidal capacitor dimensions and terminations shall meet the requirements specified by the acquiring activity (see 3.3).

3.7 Pure tin. The use of pure tin as a final finish or as an underplate is prohibited both internally and externally. Tin content of capacitor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.4).

3.8 Capacitance. The individual item requirements as measured by 4.7.4 shall be as specified by the acquiring activity (see 3.3).

3.9 Dissipation factor. When determined as specified in 4.7.5, the dissipation factor shall not exceed 2.5 percent for BX and BR, and 0.15 percent for BP.

3.10 Dielectric withstanding voltage. Capacitors shall withstand the direct current (dc) potential specified in 4.7.6 without damage or breakdown.

3.11 Insulation resistance. When measured as specified in 4.7.7, the insulation resistance shall not be less than the value specified:

At 25°C: 100,000 megohms or 1,000 megohm-microfarads, whichever is less.

At 125°C: 10,000 megohms or 100 megohm-microfarads, whichever is less.

3.12 Destructive physical analysis. When examined as specified in 4.7.8, capacitors shall meet the requirements of EIA/ECA-469.

3.13 Nondestructive internal examination (Class S only). All capacitors shall be subjected to ultrasonic examination or some other method of nondestructive internal examination as determined by the manufacturer and approved by the acquiring activity. When capacitors are examined as specified in 4.7.1, there shall be no devices delivered that show unacceptable responses as defined in EIA/ECA-469.

3.14 Visual examination. When examined as specified in 4.7.2, capacitors shall meet the visual requirements specified in appendix A.

3.15 Thermal shock and voltage conditioning. When tested as specified in 4.7.3, capacitors shall withstand the extremes of high and low temperature without visible damage and meet the following requirements within the percent defective allowed as specified in 4.6.3:

a. Dielectric withstanding voltage (at 25°C): As specified in 3.10.

b. Insulation resistance (at 25°C): Shall not be less than the initial requirement (see 3.3 and 3.11).

c. Insulation resistance (at 125°C): Shall not be less than the initial requirement (see 3.3 and 3.11).

d. Dissipation factor: Shall not exceed the value specified (see 3.3 and 3.9).

e. Capacitance (at 25°C): Shall be within the tolerance specified (see 3.3 and 3.8).

Capacitance values no more than 5 percent or .5 picofarad (pF), whichever is greater, beyond the specified tolerance limit shall be removed from the lot but shall not be considered defective for determination of the percent defective allowed.

3.16 Solderability. When capacitors are tested as specified in 4.7.9 the immersed metallized surface shall be at least 90 percent covered with a new, smooth, solder coating. The remaining 10 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. Bare metal where the solder immersion failed to cover the original coating is an indication of poor solderability and shall be cause for failure. In case of dispute, the percent of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

3.17 Resistance to soldering heat. When tested as specified in 4.7.10, capacitors shall meet the following:

a. Insulation resistance at 25°C: Not less than the initial 25°C requirement (see 3.11).

b. Capacitance: Shall not change more than -1.0 percent to +6.0 percent from the initial measured value.

c. Dissipation factor: Shall not exceed the initial limits (see 3.9).

3.18 Voltage-temperature limits. When tested as specified in 4.7.11, the capacitance change over the specified temperature range shall not exceed the limits specified in table II. The capacitance value obtained in table VIII, step C shall be considered as the reference point.

TABLE II. Capacitance change with reference to +25°C.

Characteristic	Steps A through D of table VIII Bias = 0 volts	Steps E through G of table VIII Bias = rated voltage
BP	0 ±30 ppm/°C	0 ±30 ppm/°C
BR	±15 percent	+15, -40 percent
BX	±15 percent	+15, -25 percent

3.19 Humidity, steady state, low voltage. When tested as specified in 4.7.12, capacitors shall meet the following requirements:

a. Visual examination: No mechanical damage.

b. Dielectric withstanding voltage: As specified in 3.10.

c. Insulation resistance: Not less than 50 percent of the initial 25°C requirement specified in 3.11.

d. Capacitance: Shall not change more than ±10 percent from the initial measured value.

3.20 Life (at elevated ambient temperature). When tested as specified in 4.7.13, capacitors shall meet the following requirements: 1,000 hour limits:

a. Insulation resistance: (at 125°C): Shall be not less than the initial requirement (see 3.11).

b. Visual examination: No mechanical damage.

c. Insulation resistance (at 25°C): Shall be not less than the initial requirement (see 3.11).

d. Capacitance: Shall not change more than ±20 percent from the initial measured value.

e. Dissipation factor: Shall not exceed 2.5 percent for BR or BX characteristics, or 0.15 percent for BP characteristics.

3.21 Dielectric voltage breakdown. When tested as specified in 4.7.14, no failure shall occur. A failure is defined as a steady state current above 1 milliampere (mA).

3.22 Workmanship. Discoidal capacitors shall be processed in such a manner as to be uniform in quality and shall meet the requirements of 3.2, 3.3, 3.4, 3.5 and all performance requirements. The discoidal capacitors shall pass the visual inspection criteria as specified in 4.7.2 and shall be free of other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspection. The inspection requirements specified herein are classified as follows:

a. In-process inspection (see 4.3).

b. Group A conformance inspection (see 4.5).

c. Group B inspection (see 4.6).

4.2 Inspection conditions and reference measurements.

4.2.1 Conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the "GENERAL REQUIREMENTS" of MIL-STD-202 except relative humidity shall not exceed 75 percent. Accuracy of all test voltage measurements shall be within ±2.0 percent of the specified voltage.

4.2.2 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at 25°C ±3°C prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.2.3 Power supply. The power supply used for life testing shall have a regulation of ±2 percent or less of the specified test voltage.

4.3 In-process inspection.

4.3.1 In-process inspection. Each production lot of parts shall be inspected in accordance with table IV. The nondestructive internal examination shall be for Class S only. Other screening examinations may be applied at the option of the manufacturer as approved by the acquiring activity.

4.3.1.1 Failure of parts/lots. Parts that fail the 100 percent screens are considered rejects and shall not be considered as conforming products. Lots which fail the dielectric voltage breakdown test may be rescreened, defects removed, and the lot resubmitted to the dielectric voltage breakdown test with a new sample. If the lot fails again, the lot is considered rejected. (NOTE: Dielectric voltage breakdown is a destructive test and samples shall not be supplied as conforming product).

TABLE IV. In-process inspection.

Inspection	Requirement paragraph	Test method paragraph	Sample size
Nondestructive internal examination (Class S only)	3.13	4.7.1	100%
Visual examination	3.14	4.7.2	100%
Dielectric voltage breakdown	3.21	4.7.14	Table IX, column B

4.4 Inspection of product for delivery.

4.4.1 Class B products. Inspection of product for delivery shall consist of group A and group B inspections. The acquiring activity, at its discretion, may accept a certification of compliance with group B requirements in lieu of performing group B tests (see 6.2d).

4.4.2 Class S products. Inspection of product for delivery shall consist of group A and group B inspections.

4.4.3 Class B inspection lot. An inspection lot shall consist of all discoidal capacitors of a single design, produced under essentially the same conditions, and offered for inspection at one time.

4.4.4 Class S inspection lot. An inspection/production lot shall be of one design. As a minimum requirement, the lot shall consist of all the capacitors of a single nominal capacitance/voltage rating of one design, from the same dielectric material batch, and processed as a single lot through all the manufacturing steps on the same equipment, and identified with the same date and lot code designation. The lot may contain all available capacitance tolerances for the nominal capacitance value. In addition, the lot shall conform to the following:

a. Raw materials such as end terminations, ceramic raw materials, binders, and electrode ink shall be traceable to the same lot or batch and be from the same contractor.

b. A lot number shall be assigned before electrode printing (inking) and be manufactured from the same slurry and cast on the same belt or comparable equipment.

c. A single mix of a basic ceramic formulation fired through one kiln with one temperature profile during the process, with constant dielectric design, with, in general, no more than 20 percent variation in the number of active dielectrics being assembled in one continuous buildup. Sublots may be allowed to provide a spread in capacitance value to improve the yield. This will normally be done in the case of tight tolerances and low capacitance. In these circumstances, more than 20 percent variation in the number of active dielectrics may be required.

d. End termination material shall be consistent in formulation and traceable to a single batch and shall be fired in the same kiln with no temperature adjustment during the process. All parts shall enter the kiln in one continuous operation/run for end termination firing.

e. Lot identity shall be maintained from the time the lot is assembled to the time it is accepted.

f. The lot date code (LDC) shall be recorded after firing and after end termination firing.

4.5 Group A conformance inspection. Group A inspection shall consist of the tests specified in table V. Subgroup 1 tests shall be performed on 100 percent of the product supplied under this specification to the extent specified. Failure to meet PDA requirements shall cause the lot to be rejected. Unless otherwise specified, the PDA for class B shall be 5 percent and the PDA for class S shall be 3 percent. (NOTE: During the last 25 percent of the test cycle of voltage conditioning for class S, the PDA shall not exceed 0.1 percent). For subgroup 2, a sample of parts from each inspection lot shall be randomly selected in accordance with column "A" of table IX. There shall be no failures allowed. For subgroup 3, a sample of parts from each inspection lot shall be selected at random in accordance with table VII. If the number of rejects exceed the number allowed in table VII, the sample shall be considered to have failed.

TABLE V. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sample size
Subgroup 1			
Thermal shock and voltage conditioning	3.15	4.7.3	100 %
Dielectric withstanding voltage	3.10	4.7.6	
Insulation resistance at 25°C	3.11	4.7.7	
Insulation resistance at 125°C	3.11	4.7.7	
Capacitance	3.8	4.7.4	
Dissipation factor	3.9	4.7.5	
Subgroup 2			
Visual and mechanical examination: material, physical dimensions, design and construction, marking, and workmanship	3.14, 3.22	4.7.2	See table IX, column A
Subgroup 3			
Destructive physical analysis	3.12	4.7.8	See table VII

4.6. Group B inspection. Group B inspection shall consist of the tests specified in table VI in the order shown. For class B discoidal capacitors, the group B inspection shall be made on sample units selected at random from the inspection lot or lots which have passed group A inspection. The sample shall be representative of production for each nominal size produced. For class S discoidal capacitors, the group B inspection shall be performed on sample units selected at random from the inspection lot that has passed group A inspection.

4.6.1 Sampling plan.

4.6.1.1 Class B discoidal capacitors. Sample units of the highest capacitance value produced for each voltage rating shall be submitted in accordance with table VI. The samples shall be divided into groups as specified in table VI and subjected to the specified tests.

4.6.1.2. Class S discoidal capacitiors. Samples shall be submitted for group B inspection in accordance with table VI. The samples shall be divided into groups as specified in table VI and subjected to the specified tests.

4.6.2 Failures. If the number of failures exceed the number allowed in table VI, the sample shall be considered to have failed.

4.6.3 Disposition of sample units. Sample units that have been subjected to group B inspection shall not be delivered on the contract or purchase order.

TABLE VI. Group B inspection.

Inspection	Requirement paragraph	Test method paragraph	Sample size		Number of failures allowed
			Class B	Class S	
Subgroup 1 Humidity, steady state, low voltage	3.19	4.7.12	10	12	0
Subgroup 2 Voltage/temperature limits	3.18	4.7.11	25	12	0
Subgroup 3 Solderability Resistance to soldering heat	3.16 3.17	4.7.9 4.7.10	5	12	0
Subgroup 4 Life	3.20	4.7.13	25	1/	2/ 0

1/ Sample size for class S is as follows:

Lot size	Sample size
1 - 1,200	25
1,201 - 10,000	80

2/ For class S: Sample size of 80, 1 failure allowed.

4.6.4 Noncompliance. If a sample fails to pass group B inspection, the manufacturer shall immediately notify the acquiring activity and preparing activity of this document of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the acquiring activity and preparing activity, has been taken. After the corrective action has been taken, group B inspection shall be repeated on additional sample units (all inspections, or the inspection which the original sample failed, at the option of the acquiring and preparing activity). Group A (and group B if applicable) inspection may be reinstituted; however, final acceptance shall be withheld until the group B inspection has shown that the corrective action was successful. In the event of failure after inspection, information concerning the failure and corrective action taken shall be furnished to the acquiring activity and preparing activity.

4.7 Methods of inspection.

4.7.1 Nondestructive internal examination (Class S only) (see 3.13). When specified, capacitors shall be subjected to ultrasonic examination or some other method of nondestructive internal examination approved by the acquiring activity that allows the capacitors to meet the requirements of EIA/ECA-469. The following details shall also be followed:

a. The ultrasonic test equipment shall be cleaned and maintained in accordance with the test equipment manufacturer's instructions.

b. The test facility shall establish a setup and operating procedure in accordance with the applicable test equipment manufacturer's instructions. Testing shall be done in accordance with the test equipment manufacturer's instructions and the test facility's operating procedures.

c. Each facility shall have a responsible person who has successfully completed a nondestructive testing course for the ultrasonic test equipment. The ultrasonic test equipment shall not be operated by anyone who has not been certified and instructed in the use of ultrasonic testing by the designated person. The responsible person shall prepare a test method that describes the general procedures, requirements, and techniques for ultrasonic scanning of ceramic chips.

d. Two previously determined bad capacitors of the same dielectric material and size of the parts under test shall be added to the lot for testing.

e. The test facility shall maintain adequate verification of the results of the ultrasonic examination.

4.7.2 Visual examination (see 3.14). Capacitors shall be examined under magnification as specified in appendix A and shall meet the visual requirements of appendix A.

4.7.3 Thermal shock and voltage conditioning (see 3.15). Capacitors shall be subjected to the tests of 4.7.3.1 and 4.7.3.2.

4.7.3.1 Thermal shock (see 3.15). Capacitors shall be tested in accordance with method 107 of MIL-STD-202. The following details shall apply:

a. Test condition A, except that in step 3, sample units shall be tested at +125°C.

b. Class S - 20 cycles of thermal shock; Class B - 5 cycles of thermal shock.

4.7.3.2 Voltage conditioning (see 3.15). Capacitors shall be tested in accordance with 4.7.3.2.1 or 4.7.3.2.2. The lot traveler shall indicate which test is used. When the optional voltage conditioning test of 4.7.3.2.2 is used, the traveler shall include the specific accelerated voltage used and the test time (see figure 1).

4.7.3.2.1 Standard voltage conditioning. Voltage conditioning shall be started after completion of the thermal shock test. The voltage conditioning shall consist of applying twice the rated voltage to the units at the maximum rated temperature of 125°C +4°C, -0°C, for a minimum of 168 hours and a maximum of 264 hours for class S product, and 164 hours ±4 hours for class B product. The voltage conditioning for class S capacitors may be terminated at any time during the 168 hour to 264 hour time interval provided that failures (blown fuses or less than 95 percent voltage) do not exceed 0.1 percent or one unit during the last 48 hours. Voltage shall be applied and shall reach maximum value within one second, maximum. To assure that at least 95 percent of the applied test voltage is maintained for the duration of the exposure period, the circuit on figure 1 shall be used. After completion of the exposure period, the unit shall be allowed to stabilize at room temperature (25°C) (for no more than one hour). After stabilization at room temperature, the dielectric withstanding voltage and insulation resistance shall be measured as specified in 4.7.6 and 4.7.7, respectively. After measurement of dielectric withstanding voltage and insulation resistance at 25°C, the unit shall be stabilized at maximum rated temperature and insulation resistance measured. After allowing the unit to stabilize at room temperature for 10 hours minimum, the capacitance and dissipation factor shall be measured as specified in 4.7.4 and 4.7.5, respectively. If the voltage conditioning test is performed with individual fuses in series with each part, any part tested in a position where a fuse fails shall be tested for insulation resistance and dielectric withstanding voltage. If the part meets the initial requirements for insulation resistance and dielectric withstanding voltage, the part shall be rejected but shall not be counted against the percent defective allowed.

4.7.3.2.2 Optional voltage conditioning. The manufacturer, with approval from the acquiring activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning test of 4.7.3.2.1. All conditions of 4.7.3.2.1 apply, with the exception of the voltage applied and test time. The minimum time duration, $T_{(test)}$, shall be calculated as follows:

$$T_{test}\ (min.) = \frac{1344}{(E_{test} / E_{rated})^3}$$

Where: $2 \times E_{rated} \le E_{test} \le 4 \times E_{rated}$

E_{test} = Applied voltage

E_{rated} = Rated voltage of the capacitor

T_{test} (min.) = Minimum test time in hours

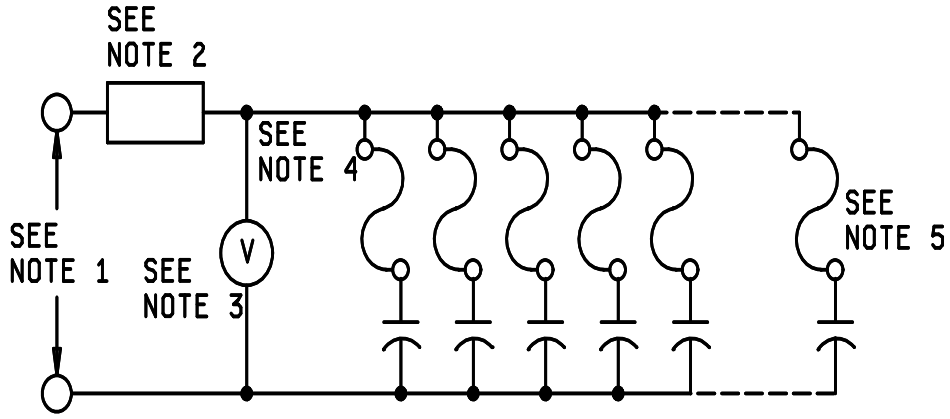
NOTE: This optional voltage conditioning test may not be used on capacitors with voltage ratings greater than 200 volts.

4.7.4 Capacitance (see 3.8). Capacitors shall be tested in accordance with method 305 of MIL-STD-202. The following details and exceptions shall apply:

a. Test frequency: 1 MHz ±100 KHz when the nominal capacitance is 100 pF or less, and 1 KHz ±100 Hz when the nominal capacitance is greater than 100 pF.

b. Voltage: A root-mean-square potential (RMS) of 1.0 volt ±0.2 volt for 1 KHz measurements and less than 1.0 volt for 1 MHz measurements.

NOTE: Following a dielectric withstanding voltage or insulation resistance test, capacitance measurement may be delayed for a period of up to 24 hours.



NOTES:
1. The power supply shall be capable of providing a minimum of twice the rated voltage of the capacitors at a fault current of 30 mA minimum.
2. The current limiting device shall be a resistor and/or a fuse. The current shall be limited to no less than 30 mA and no more than 10 A.
3. There shall be a voltage monitor that will trigger an alarm and shut off the test if the applied voltage drops by more than 5 percent.
4. Fuses shall be optional and resistors shall not be allowed. If fuses are used, the total resistance of the fuse, connections, and the connecting wires shall not exceed 50 ohms at +125°C.
5. The capacitor bank shall be no less than 10.

FIGURE 1. Voltage conditioning circuitry.

4.7.5 Dissipation factor (see 3.9). The dissipation factor shall be measured with a capacitance bridge or other suitable method at the frequency and voltage specified in 4.7.4. The inherent accuracy of the measurement shall be ±2 percent of the reading plus 0.1 percent dissipation factor (absolute) unless otherwise specified. Suitable measurement techniques shall be used to minimize errors due to the connections between the measuring device and the capacitor.

4.7.6 Dielectric withstanding voltage (see 3.10). Capacitors shall be tested in accordance with method 301 of MIL-STD-202. The following details shall apply:

a. Magnitude and nature of test voltage: 250 percent of the dc rated voltage.

b. Duration of application of test voltage: 5 seconds ±1 second. The test voltage shall be raised from zero to the specified value within 1 second, maximum.

c. Points of application of test voltage: Between the capacitor element terminals.

d. Limiting value of surge current: Shall be limited between 30 mA and 50 mA.

e. Examination after test: Capacitors shall be examined for evidence of damage or breakdown.

4.7.7 Insulation resistance (see 3.11). Capacitors shall be tested in accordance with method 302 of MIL-STD-202. The following details shall apply:

a. Test potential: Rated voltage.

b. Special conditions: If failure occurs at a relative humidity above 50 percent, the insulation resistance may be measured again at any relative humidity less than 50 percent.

c. Points of measurements: Between the inner and outer terminations.

4.7.8 Destructive physical analysis (see 3.3, 3.4, and 3.12). Capacitors shall be examined as specified in EIA/ECA-469, 4.7.8a through 4.7.8k, inclusive, and in accordance with table VII.

a. Chipping of termination edge (see figure 2A) shall be cause for rejection if it will hinder uniform metallization or if it extends to or is near (within 3 mils (0.076 mm)) an electrode plate.

b. Number of electrodes shall correspond to the electrode number specified for each lot. Variation of number of electrodes shall be acceptable from lot to lot.

c. Thin covers less than 3 mils (0.076 mm) are cause for rejection.

d. Borders or edges (see figure 2B) that are less than 3 mils (0.076 mm) from a plate shall be cause for rejection.

e. Electrode shorts (see figure 2C) shall be cause for rejection.

f. Dielectric thickness of any single layer shall not be reduced by more than 50 percent of its mean thickness (see figure 2D) for any reason, including voids, accumulative affects of voids, or curvature.

g. Discontinuities in the electrodes, if not by design, shall not extend to more than 20 percent of the section (see figure 2F).

h. Isolated electrodes or electrode fragments connected to the termination are not to be subject to rejection if separated from other active conductors by at least the nominal dielectric thickness of that capacitor design (see figure 2G).

i. Delaminations and defects within the active area of the electrodes shall not exceed 30 percent of the active length of the electrodes or 10 mils (0.254 mm), whichever is greater, and shall not reduce the dielectric more than 50 percent. No more than three such defects shall appear in a single capacitor examined.

j. Delaminations shall be permitted in the margin area (see figure 2H).

k. There shall be contact between the electrodes and the metallization.

TABLE VII. Destructive physical analysis sample sizes.

Lot size	Class S and Class B Minimum sample size	Rejects allowable class S	Rejects allowable class B
1 - 500	14	0	0
501 - 1,200	20	0	1
1,201 - 10,000	32	1	2

4.7.9 Solderability (see 3.16). Capacitors shall be tested in accordance with method 208 of MIL-STD-202. The following details and exceptions shall apply:

a. Solder shall be Pb36 in accordance with J-STD-006.

b. Each capacitor shall be completely immersed.

c. The method of attaching the capacitor to the dipping apparatus shall be so designed as to expose 100 percent of the inner termination and 100 percent of the outer termination.

d. Examination of terminations shall be in accordance with 3.16.

4.7.10 Resistance to soldering heat (see 3.17). Capacitors shall be tested in accordance with method 210 of MIL-STD-202. The following details shall apply:

a. Test condition B, except the solder temperature shall be 230°C +5°C, -0°C and the duration shall be 5 seconds +1 second, -0 second. Each capacitor shall be completely immersed twice.

b. Cooling time prior to measurement after test: 10 minutes minimum and up to 24 hours maximum.

c. Measurements before test: Capacitance, dissipation factor, and insulation resistance at 25°C shall be measured and recorded as specified in 4.7.4, 4.7.5, and 4.7.7, respectively.

d. Measurement after test: Capacitance, dissipation factor, and insulation resistance at 25°C shall be measured and recorded as specified in 4.7.4, 4.7.5, and 4.7.7, respectively.

4.7.11 Voltage-temperature limits (see 3.18). The temperature of each capacitor shall be varied as specified in table VIII. Capacitance measurements shall be made at the frequency and voltage specified in 4.7.4. The dc rated voltage specified in table VIII shall be maintained on the capacitor during step E to step G inclusive. Capacitance measurements shall be made at each step specified in table VIII and at five intermediate temperatures between step B and step G to establish a true characteristic curve. Capacitors shall be kept at each temperature until temperature equilibrium is attained.

4.7.11.1 Voltage-temperature limits for conformance inspection. Capacitance measurements shall be made only for steps C, D, E, and G of table VIII.

TABLE VIII. Voltage-temperature limit cycle.

Step	Voltage, dc	Temperature °C
A	None	+25 ±2
B	None	-55 ±2
C (reference)	None	+25 ±2
D	None	+125 ±2
E	Rated	+125 ±2
F	Rated	+25 ±2
G	Rated	-55 ±2

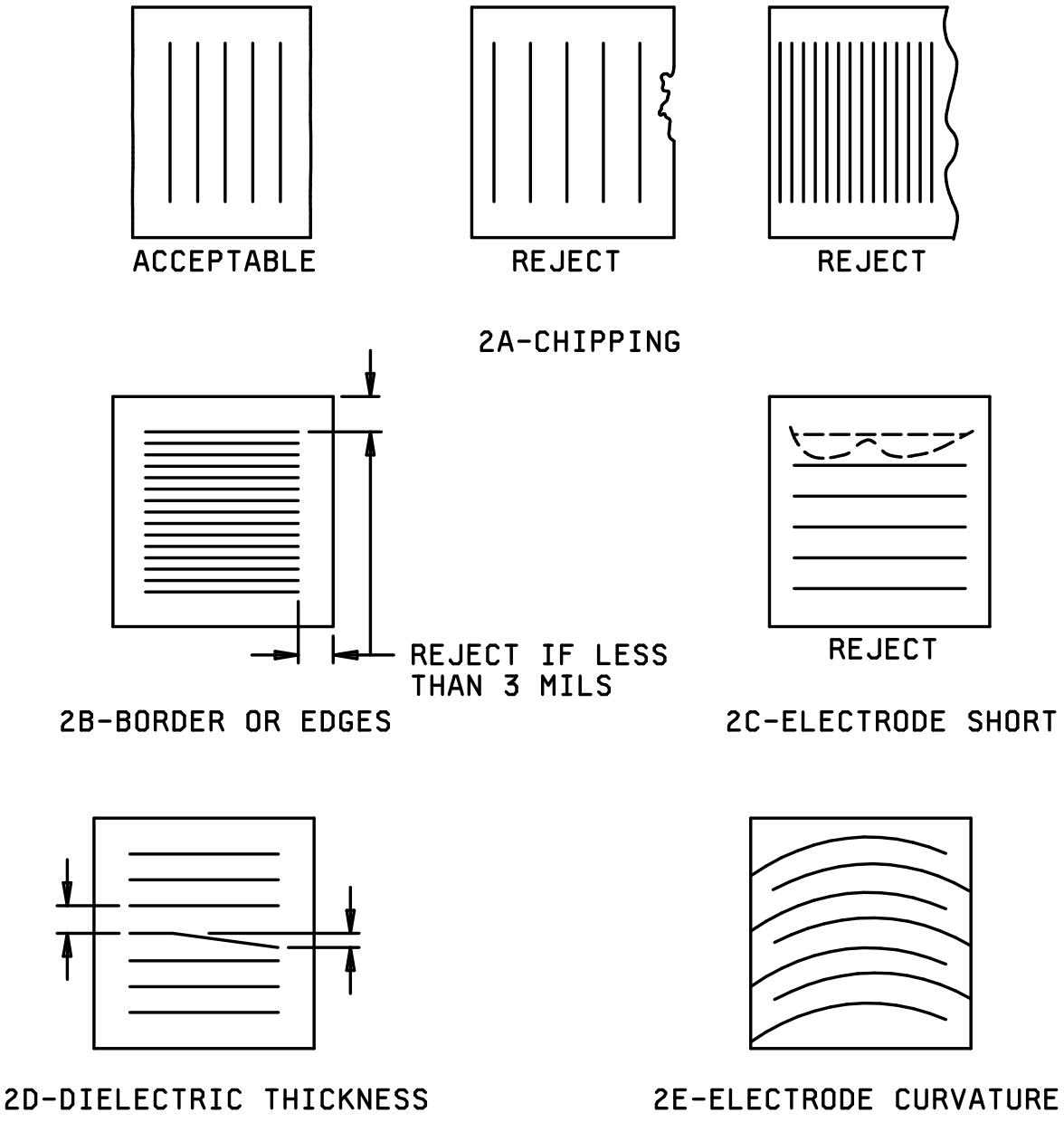
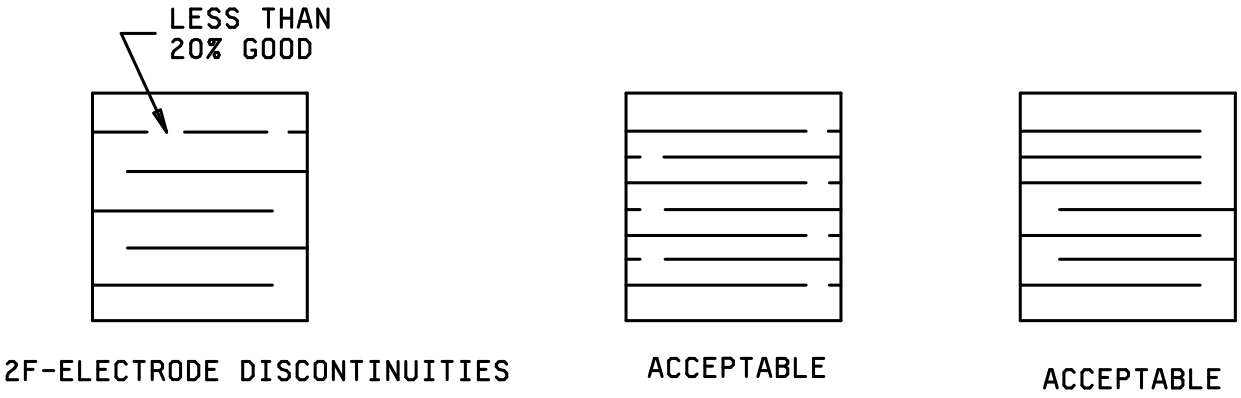
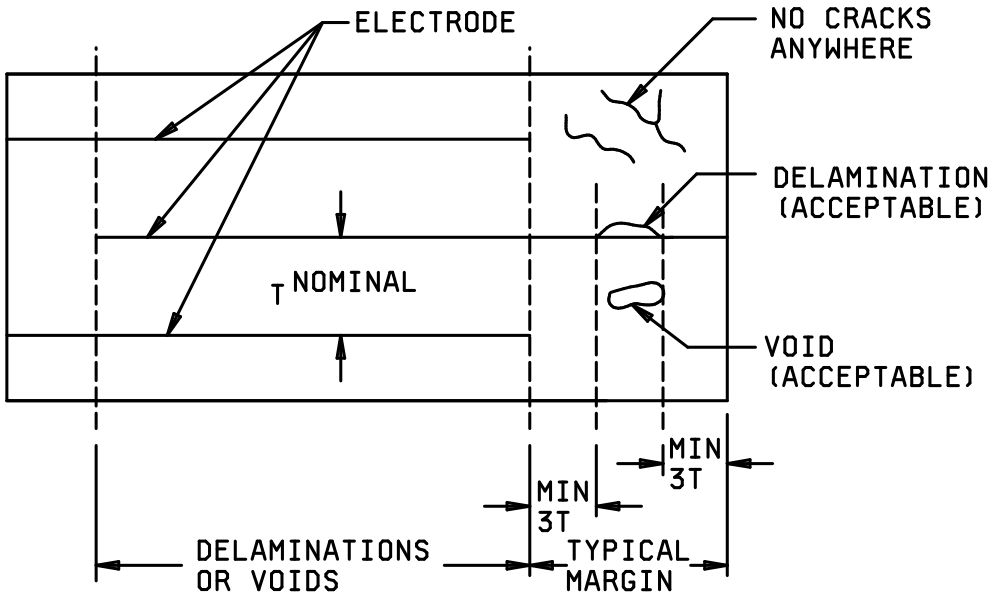


FIGURE 2. Sectioned capacitors (only one side of discoidal is shown).



2G-ISOLATED ELECTRODES



2H-VOIDS AND DELAMINATIONS

FIGURE 2. Sectioned capacitors (only one side of discoidal is shown) - Continued.

4.7.12 Humidity, steady state, low voltage (see 3.19). Capacitors shall be tested in accordance with method 103 of MIL-STD-202, test condition A. The following details and exceptions shall apply:

NOTE: At no time during test shall voltage greater than 1.5 volts be applied to any capacitor under test.

a. Initial measurements: Capacitance.

b. Tests: Capacitors shall be subjected to an environment of 85°C with 85 percent humidity for 240 hours minimum. Cycling shall not be performed. A dc potential of 1.3 volts ±0.25 volts maximum shall be applied continuously through a 100 kilohm resistor to each device under test.

c. Final measurements: Upon completion of above tests, remove capacitors from chamber and allow to dry and stabilize at 25°C before performing measurements for capacitance, dissipation factor, and insulation resistance through a 100 kilohm resistor at 1.5 volts maximum, in accordance with 3.8, 3.9, and 3.11.

d. Visual examination: After final measurements, the capacitor shall be examined for evidence of mechanical damage and obliteration of marking.

4.7.13 Life (at elevated ambient temperature) (see 3.20). Capacitors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

a. Distance of temperature measurements from specimens is not applicable.

b. Test temperature tolerance: +125°C +4°C, -0°C.

c. Capacitors shall be subjected to the voltage and circuit specified in 4.7.3.2.

d. Test duration: 1,000 hours.

e. Measurements during and after exposure: At the conclusion of 1,000 hours and while the capacitors are at the applicable high-test temperature, the insulation resistance shall be measured as specified in 4.7.7. At the option of the manufacturer, the units may be immediately transferred (period of transfer not to exceed 15 minutes) to another chamber maintained at the same temperature for the purpose of measuring the insulation resistance. The insulation resistance measurement shall be made only after the units have stabilized at the test temperature. The capacitors shall then be returned to the inspection conditions specified in 4.4 and shall be visually examined for evidence of mechanical damage; capacitance, dissipation factor, and insulation resistance shall be measured as specified in 4.7.4, 4.7.5, and 4.7.7.

4.7.14 Dielectric voltage breakdown (see 3.21). Each discoidal capacitor in the sample shall be placed in an oil (or other suitable dielectric fluid) bath and connected in series with an instrument to measure current (must be able to measure mA). A dc voltage shall be gradually applied at no greater than 50 volts per second until failure occurs. A failure is defined as a steady state current above 1 mA. No failure shall occur at an applied voltage of less than 6X rated voltage or 1,200 V dc, whichever is less.

TABLE IX. C = 0 sampling plan. 1/

Lot size	Sample size	
	A	B
1 - 5	100 percent	100 percent
6 - 19	100 percent	5
20 - 50	20	5
51 - 90	20	7
91 - 150	20	11
151 - 280	20	13
281 - 500	47	16
501 - 1,200	47	19
1,201 - 3,200	53	23
3,201 - 10,000	68	29
10,001 - 35,000	77	35
35,001 - 150,000	96	40

1/ The acceptance number in all cases is zero.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2c). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The discoidal capacitors described in this specification are primarily intended for use in EMI/RFI filters covered by MIL-PRF-28861.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this specification.

b. Engineering item requirements (see 6.3).

c. Packaging requirements (see 5.1).

d. Whether the manufacturer performs the group B test for class B discoidals or provides certification of compliance with group B requirements.

6.3 Engineering item requirements. Engineering item requirements should specify the following:

a. Product level.

b. Capacitance value.

c. Capacitance tolerance.

d. Outer diameter.

e. Voltage rating.

f. Dissipation factor.

g. VTL characteristic (e.g. - BP, BR, or BX).

6.4 Tin whisker growth. Tin plating is prohibited (see 3.7) because it may result in tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM B545 (Standard Specification for Electrodeposited Coating of Tin).

6.5 Definitions. The following terms have been used in this specification and are defined as stated herein.

6.5.1 Chip (see figure 3A). Any place where material has been removed as a result of a fracture.

6.5.2 Crack (see figure 3B). Any fissure or parting of the material.

6.5.3 Delamination (see figure 3G). The separating of capacitor layers.

6.5.4 Etching (see figure 3E). Thin markings or lines in a surface.

6.5.5 Metallization (see figure 3H). A palladium silver, silver, or solder coated termination.

6.5.6 Pinhole (see figure 3F). A minuscule circular hollow or cavity in a body no larger than 2 mils (0.051 mm) in diameter and no deeper than 2 mils (0.051 mm).

6.5.7 Ripple (see figure 3D). A wave in a surface; defined as being 3 mils (0.076 mm) or more in amplitude and 1 mil (0.025 mm) or more in width.

6.6.8 Striation (see figure 3C). Thin grooves, channels, or lines running in or on the surface of the body.

6.7 Environmentally preferable material. Environmentally preferable materials should be used to the maximum extent possible to meet the requirements of this specification. As of the dating of this document, the U.S. Environmental Protection Agency (EPA) is focusing efforts on reducing 31 priority chemicals. The list of chemicals is available on their website at http://www.epa.gov/osw/hazard/wastemin/priority.htm. Included in the EPA list of 31 priority chemicals are cadmium, lead, and mercury. Use of these materials should be minimized or eliminated unless needed to meet the requirements specified herein (see section 3).

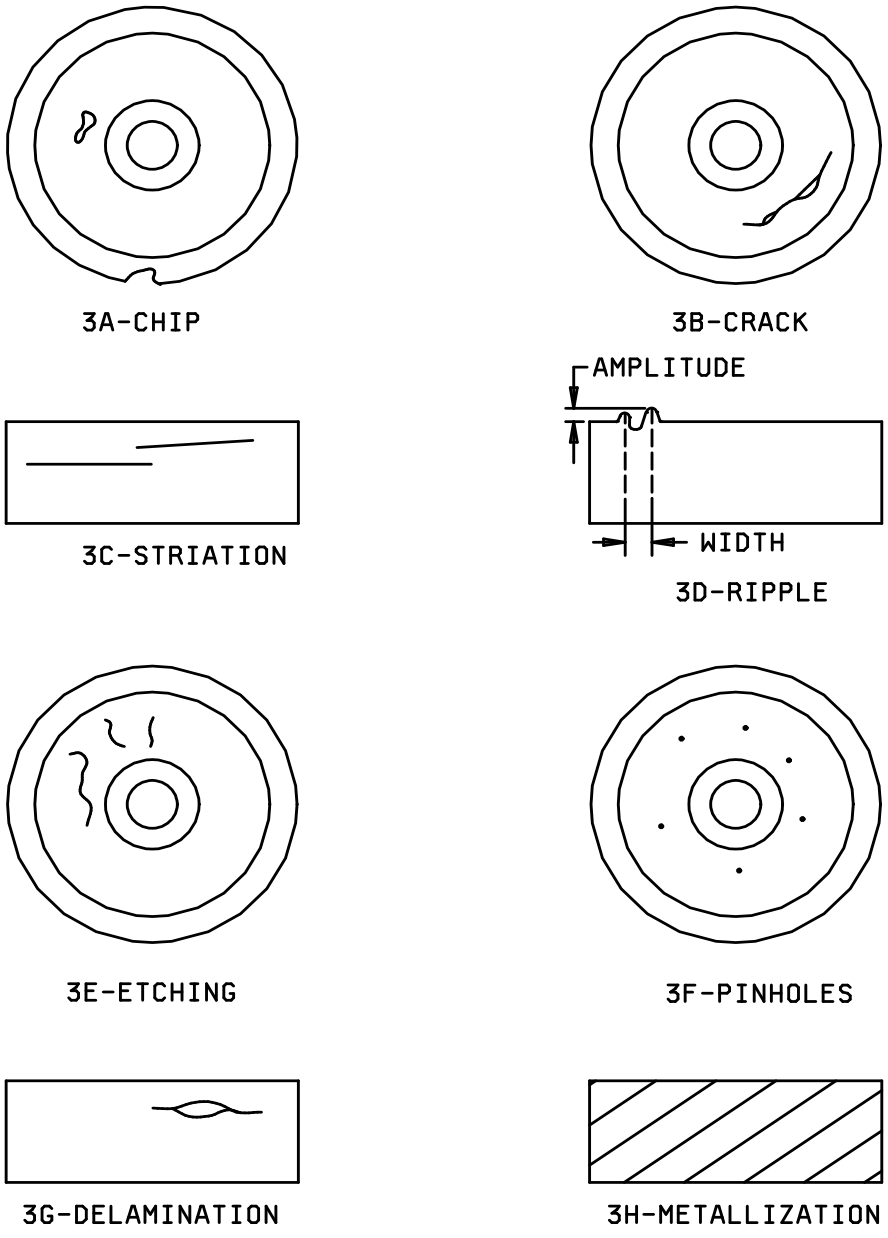


FIGURE 3. Definitions.

6.8 Subject term (key word) listing.

Capacitance
EMI
Filter
RFI

6.9 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

APPENDIX A

VISUAL INSPECTION CRITERIA FOR DISCOIDAL CAPACITORS

A.1 SCOPE

A.1.1 Scope. This appendix specifies the visual inspection criteria for discoidal capacitors. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance only.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 TEST EQUIPMENT

A.3.1 Apparatus. The apparatus for this inspection shall include optical equipment capable of 10 power magnification and any other visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination.

A.4 INSPECTION

A.4.1 Procedure. The device shall be examined under 10 power magnification to determine compliance with the requirements specified herein. The order in which criteria is presented is not a required order of examination of the terminations prior to sectioning. The samples shall be sectioned perpendicular to the plate surface to expose the internal electrodes. If a visual inspection requirement is in conflict with the detail standard, the latter shall govern.

A.4.1.1 Rejection criteria. Devices that deviate from the material, design, or construction requirements specified or exhibit any of the following defects shall be unacceptable.

A.4.1.1.1 Termination metallization (silvering or soldering).

a. End terminals shall be 80 percent covered with metallization.

b. Pinholes (see figure A-1A) shall not cover more than 5 percent of metallization or be larger than 5 mils (0.127 mm) in diameter.

c. There shall be no cracks in the metallization.

d. The inside edge of metallization (see figure A-1B) shall be separated from the opposite termination metallization by a minimum of one third the total radius of the discoidal.

e. Overlap (see figure A-1C) shall be continuously smooth, without sharp points greater than one third the unmetallized radius.

f. No single gap in the overlap shall exceed 10 percent of the overlap area (see figure A-1D). Combination of all gaps shall not reduce the solderable surface (outer diameter) to less than 240 degrees.

g. Buildup of overlap (see figure A-1E) shall not exceed 10 mils (0.254 mm).

h. There shall be no lifting of the metallization (see figure A-1F).

i. The overlap shall be as specified.

j. There shall be no foreign material adhering to the solder.

k. Metallized edges shall not be reduced to less than 90 percent due to chipping or the metallization process.

APPENDIX A

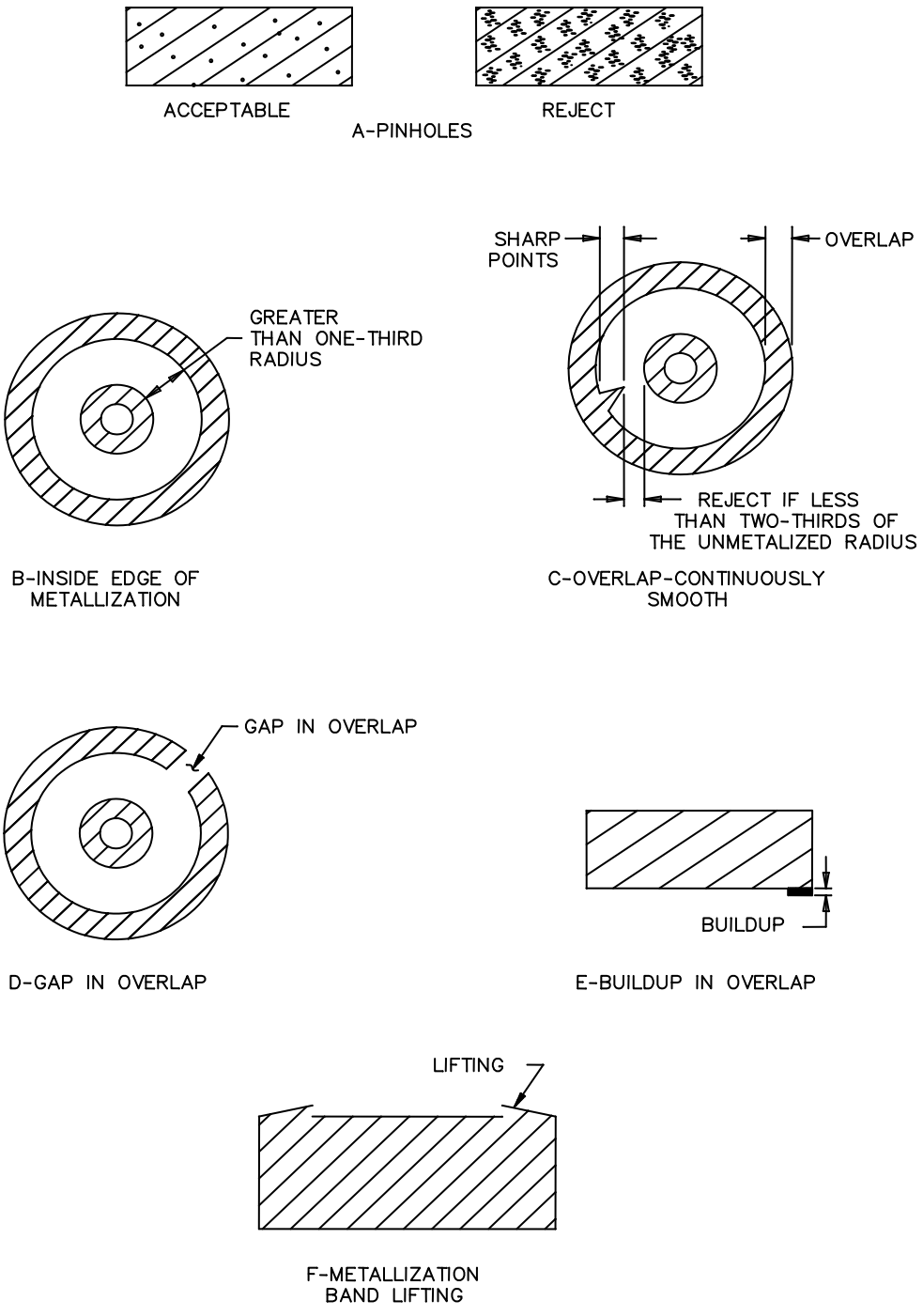


FIGURE A-1. Termination metallization inspection.

A.4.1.1.2 Capacitor surface examination (after termination).

a. There shall be no cracks in the capacitor body.

b. No chips shall be greater that 10 mils (0.254 mm) in diameter or deeper than 3 mils (0.076 mm); these chips shall not cover more than 20 percent of a surface. No internal electrode shall be exposed through the cover.

c. Rough or finely chipped edges are not permitted (see figure A-2).

d. Fused dust or excess material on cover which prevents a capacitor from lying flat shall be cause for rejection. Lumps, burrs, fused cutting dust, or excess dielectric material shall not be greater than 5 mils (0.127 mm) in diameter and may not protrude more than 10 mils (0.254 mm) out of surface; they shall not cover more than 20 percent of a surface.

e. Indications of bubbles in dielectric material (such as circular shadows) shall be cause for rejection.

f. Striations are unacceptable.

g. Warpage, exceeding 5 mils (0.127 mm), or twisting of body shall be cause for rejection.

h. Pinholes shall not cover more than 10 percent of the surface (see figure 5) and be no larger than 2 mils (0.051 mm) in diameter.

i. Etching in a cover is permitted provided it does not exceed in depth more than 3 mils (0.076 mm).

j. A uniform rough surface is permitted provided that it cannot be identified as a collection of ripples.

k. There shall be no delamination of dielectric layers.

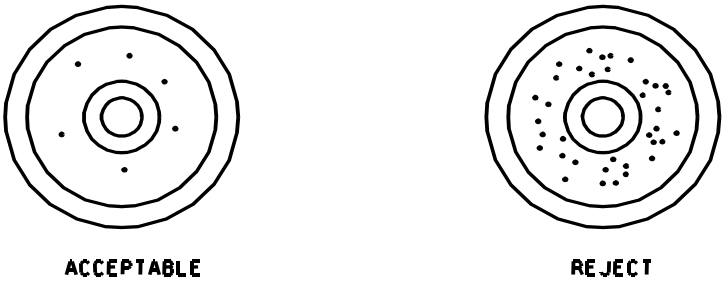


FIGURE A-2. Pinholes.

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC
NASA - NA

Preparing activity:
DLA - CC

(Project 5910-2009-047)

Review activities:
Army - AR, AT, AV, MI
Navy - AS, MC, OS, SH
Air Force - 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using ASSIST Online database at https://assist.daps.dla.mil.